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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 10/582,833  
Filing Date: June 14, 2006  
Appellant(s): PEKKARINEN ET AL.

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Keith R. Obert  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed on July 2, 2010 appealing from the Office action mailed December 8, 2009.

**(1) Real Party in Interest**

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The following is a list of claims that are rejected and pending in the application:

1-20

**(4) Status of Amendments After Final**

No amendment after final has been filed.

**(5) Summary of Claimed Subject Matter**

The examiner has no comment on the summary of claimed subject matter contained in the brief.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

### **WITHDRAWN REJECTIONS**

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner: Claims 1-20 rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement; Claims 1-20 rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

### **(7) Claims Appendix**

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

### **(8) Evidence Relied Upon**

4,303,960	Sherwood et al.	December 1981
5,889,308	Hong et al.	March 1999
6,175,394 B1	Wu et al.	January 2001

### **(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims: Claims 1, 4, 5, 8, 11, 12, 15, 16, 19, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hong et al (US Patent 5,889,308).

1. Regarding claim 1, Hong teaches a semiconductor component, comprising a semiconductor element (layer 102 in fig. 4) encased by a cover element (element a) having an integrated electroconductive metal element (layer 105) comprising at least one outlet, wherein the at least one outlet is configured to *constantly* connect the

electroconductive metal element to ground in order to shield the semiconductor element against electrostatic pulses (column 4, lines 43-57).

2. Regarding claim 4, Hong teaches a semiconductor component according to claim 1, wherein the electroconductive metal element forms a permanent, integrated part of the semiconductor component (see fig. 4).

3. Regarding claim 5, Hong teaches a semiconductor component according to claim 4 claim 1, wherein the electroconductive metal element (layer 105) is placed underneath the cover element of the semiconductor component, inside said cover element (element a in fig. 4).

4. Regarding claim 8, Hong teaches a method for shielding a semiconductor element against electrostatic pulses, comprising: integrating the semiconductor element in a semiconductor component (layer 102 in fig. 4), covering the semiconductor element with a cover element (element a), integrating an electroconductive metal element (layer 105) within the cover element of the semiconductor component and providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to *constantly* connect the electroconductive metal element to ground (column 4, lines 43-57).

5. Regarding claim 11, Hong teaches a method according to claim 8, wherein the electroconductive metal element is integrated as a permanent part of the semiconductor component (see fig. 4).

6. Regarding claim 12, Hong teaches a method according to claim 11, wherein the electroconductive metal element is integrated underneath the cover element of the semiconductor component, inside said cover element (see fig. 4).

7. Regarding claim 15, Hong teaches an arrangement including a mounting tray and at least one semiconductor component, wherein said at least one semiconductor component comprises a semiconductor element (layer 102 in fig. 4) encased by a cover element (layer a) having an integrated electroconductive metal element (layer 105), where the electroconductive metal element is provided with at least one outlet that is *constantly* grounded to a ground plane of the mounting tray (column 4, lines 43-57).

8. Regarding claim 16, Hong teaches apparatus for shielding a semiconductor element against electrostatic pulses, comprising: means for covering (layer a in fig. 4) the semiconductor element in a semiconductor component (layer 102) having an integrated electroconductive metal element (layer 105); and means for providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to connect the electroconductive metal element to ground (column 4, lines 43-57).

9. Regarding claim 19, Hong teaches the apparatus of claim 16, wherein the electroconductive metal element is integrated as a permanent part of the semiconductor component (see fig. 4).

10. Regarding claim 20, Hong teaches the apparatus of claim 16, wherein the electroconductive metal element is integrated underneath the cover element of means for covering the semiconductor component, inside said cover element (see fig. 4).

11. Claims 1, 2, 4-9,11-14,16, 17,19, 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sherwood et al (US Patent 4,303,960).
12. Regarding claim 1, Sherwood teaches a semiconductor component, comprising a semiconductor element (MOS in layer 103 in fig. 3) encased by a cover element (encased by layer 22 in fig. 1 and the substrate the MOS is formed) having an integrated electroconductive metal element (layer 75) comprising at least one outlet, wherein the at least one outlet is configured to connect the electroconductive metal element to ground in order to shield the semiconductor element against electrostatic pulses (column 4, lines 59-65).
13. Regarding claim 2, Sherwood teaches a semiconductor component according to claim 1, wherein in structure, the electroconductive metal element is a planar sheet (column 3, lines 43-46).
14. Regarding claim 4, Sherwood teaches a semiconductor component according to claim 1, wherein the electroconductive metal element forms a permanent, integrated part of the semiconductor component (see fig. 1).
15. Regarding claim 5, Sherwood teaches a semiconductor component according to claim 4 claim 1, wherein the electroconductive metal element (layer 75 in figs 1 and 3) is placed underneath the cover element (when "the cover element" in claim 1 is interpreted as to be formed by layers 21 and 22) of the semiconductor component, inside said cover element.

16. Regarding claim 6, Sherwood teaches a semiconductor component according to claim 1, wherein the electroconductive metal element (layer 75 in fig. 3) is placed on top of attached to the cover element of the semiconductor component, outside said cover element (layer 75 is outside of "the cover element" formed by layer 22 and the substrate the MOS is formed (layer 103)).

17. Regarding claim 7, Sherwood teaches a semiconductor component according to claim 1, wherein the electroconductive metal element is induced in the cover element of the semiconductor component either chemically or electrochemically (column 3, lines 43-52, where Sherwood teaches using glue to bond layer 75 to the device. The bonding force of the glue is generated by molecular force of the glue—thus, induced chemically). Also, how the electroconductive metal element is formed, whether chemically, electrochemically, or other process, does not carry patentable weight in a device claim. “[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.” In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP 2113.

18. Regarding claim 8, Sherwood teaches a method for shielding a semiconductor element against electrostatic pulses, comprising: integrating the semiconductor element in a semiconductor component (MOS in layer 103, see fig. 3), covering the

semiconductor element with a cover element (cover element formed by layers 22 and layer 103), integrating an electroconductive metal element (layer 75 in figs. 1 and 3) within the cover element of the semiconductor component and providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to connect the electroconductive metal element to ground (column 4, lines 59-65).

19. Regarding claim 9, Sherwood teaches a method according to claim 8, wherein in the semiconductor component, there is integrated an electroconductive, planar metal element (layer 75 in fig. 3).

20. Regarding claim 11, Sherwood teaches a method according to claim 8, wherein the electroconductive metal element (layer 75 see figs. 1 and 3) is integrated as a permanent part of the semiconductor component.

21. Regarding claim 12, Sherwood teaches a method according to claim 11, wherein the electroconductive metal element (layer 75 in figs. 1 and 3) is integrated underneath the cover element (when the cover element is formed by layers 21 and 22 in fig. 1) of the semiconductor component, inside said cover element.

22. Regarding claim 13, Sherwood teaches a method according to claim 11, wherein the electroconductive metal element (layer 75 in fig. 3) is integrated on top of by attachment to the cover element of the semiconductor component, outside said cover element (layer 75 is outside of the cover element formed by layer 22 and layer 103 in fig. 3).

23. Regarding claim 14, Sherwood teaches a method according to claim 8, wherein the electroconductive element is induced in the cover element of the semiconductor component either chemically or electrochemically (column 3, lines 43-52, where Sherwood teaches using glue to bond layer 75 to the device. The bonding force of the glue is generated by molecular force of the glue—thus, induced chemically).
24. Regarding claim 16, Sherwood teaches apparatus for shielding a semiconductor element against electrostatic pulses, comprising: means for covering (layers 21 and 22) the semiconductor element in a semiconductor component (MOS on layer 103) having an integrated electroconductive metal element (layer 75 in fig. 3); and for providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to connect the electroconductive metal element to ground (column 4, lines 59-65).
25. Regarding claim 17, Sherwood teaches the apparatus of claim 16, wherein in the semiconductor component, there is integrated an electroconductive, planar metal element (layer 75 in fig. 3).
26. Regarding claim 19, Sherwood teaches the apparatus of claim 16, wherein the electroconductive metal element (layer 75 in figs. 1 and 3) is integrated as a permanent part of the semiconductor component.
27. Regarding claim 20, Sherwood teaches the apparatus of claim 16, wherein the electroconductive metal element (layer 75 in figs. 1 and 3) is integrated underneath the cover element of means for covering the semiconductor component, inside said cover element.

28. Claims 1, 3, 8, 10, 16 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al (US Patent 6,175,394 B1).
29. Regarding claim 1, Wu teaches a semiconductor component, comprising a semiconductor element (layer 20 in fig. 1) encased by a cover element (cover of the display panel) having an integrated electroconductive metal element (layer 24, see column 2, lines 28-30) comprising at least one outlet, wherein the at least one outlet is configured to *constantly* connect the electroconductive metal element to ground (column 7, lines 62-65) in order to shield the semiconductor element against electrostatic pulses. Note that although the content of column 7, lines 62-65 describes fig. 9, Wu teaches that the configuration and operation of fig. 9 also apply to fig. 1 (column 7, lines 35-37).
30. Regarding claim 3, Wu teaches a semiconductor component according to claim 1, wherein the electroconductive metal element is a thin loop structure (see fig. 1).
31. Regarding claim 8, Wu teaches a method for shielding a semiconductor element against electrostatic pulses, comprising: integrating the semiconductor element (layer 20 in fig. 1) in a semiconductor component, covering the semiconductor element with a cover element (cover of the display panel), integrating an electroconductive metal element (layer 24 in fig. 1) within the cover element of the semiconductor component and providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to connect the electroconductive metal element to ground (column 7, lines 61-65).

32. Regarding claim 10, Wu teaches a method according to claim 8, wherein in the semiconductor component, there is integrated an electroconductive, loop-shaped metal element (layer 24 in fig. 1).
33. Regarding claim 16, Wu teaches apparatus for shielding a semiconductor element against electrostatic pulses, comprising: means for covering the semiconductor element in a semiconductor component (layer 20 in fig. 1) having an integrated electroconductive metal element (layer 24); and means for providing at least one outlet for the integrated electroconductive metal element, so that the at least one outlet is configured to connect the electroconductive metal element to ground (column 7, lines 61-65).
34. Regarding claim 18, Wu teaches the apparatus of claim 16, wherein in the semiconductor component, there is integrated an electroconductive, loop-shaped metal element (layer 24 in fig. 1).

#### **(10) Response to Argument**

Appellant argues on page 7 of the Brief submitted on July 2, 2010 that " Hong at least fails to disclose or suggest at least one outlet is configured to constantly connect the electroconductive metal element to ground, as recited in claim 1" since Hong's electroconductive metal element "turns into a conducting state only when a certain threshold voltage is exceeded." Even though Hong's varistor (106, which is connected to 105, in fig. 4) requires a minimum voltage to pass overcurrent, the electroconductive metal element (layer 105, which Examiner points to as the claimed electroconductive

metal element, in fig. 4) is *physically* connected (hard-wired) to ground *all the time*. Furthermore, since layer 105 is made of metal, it is *constantly* ready to conduct current and its conductivity does not depend on applied voltage level. Thus, Hong's teaching meets the claimed limitations—"...constantly connect the electroconductive metal element to ground in order to shield the semiconductor element against electrostatic pulses."

Appellant states on page 8 of the Brief that Sherwood fails to teach "an outlet...configured to constantly connect the electroconductive metal element to ground" because "the conductive surface [(layer 75, which Examiner points to as the claimed electroconductive metal element, in fig. 3)] acts as an excellent conductor in voltage more than the specific voltage and acts as an insulator below the specific voltage." Firstly, Sherwood teaches that layer 75 be made of metal such as copper (column 3, lines 43-52), which is an excellent conductor and does not act as an insulator below a specific voltage (as Appellant claims). Secondly, Sherwood teaches conductive surface 75 being *constantly* connected (hard-wired) to ground (though not directly, see column 4, lines 59-65 and figs. 1 and 5). Appellant also points out that cable 24, which connects layer 75 to ground, "can be unplugged from the plug (88)." Although Sherwood's electrostatic shield is not immune from intentional dismantlement (such as yanking cable 24 to disconnect it to ground or cutting cable 24 so that it's not connected to ground), it is intended to be *constantly* connected to ground to protect the device from static electricity--and layer 75 is physically connected to ground all the time.

Appellant states on page 9 of the Brief that "Wu does not teach that for normal operation the guard ring (130) is held at a fixed potential such as ground. Therefore, Wu does not disclose that for all operations (including normal, standby, assembly, test, etc. operations) the guard ring (130) is held at a fixed potential such as ground. Accordingly, the guard ring (130) is not configured to constantly connect to ground, since during normal operation the guard ring (130) is not held at ground." Examiner disagrees with Appellant's contention. Note that Wu teaches to constantly connect layer 24 (which Examiner points to as the claimed electroconductive metal element) to ground: not only in normal operation but also "for testing purposes" and "throughout the assembly" (column 2, lines 39-49). Furthermore, Wu teaches that guard ring 130 in fig. 9, whose configuration and operation are similar to the display shown in fig. 1 (column 7, lines 34-37), to provide the display "to a constant potential such as ground." Wu further discloses that "it is conventional to leave such an inner guard ring [guard ring 130] in place after the completion of the display and "[f]or typical assembly or test operations...the guard ring 130 is held at a fixed potential such as ground."

**(11) Related Proceeding(s) Appendix**

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Examiner, Art Unit 2826

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